Remarks

The referenced patent application has been reviewed in light of the referenced Office Action. In the Claims, claims 1-28 are pending in the referenced application. Claims 1, 10, 15, and 20 are amended in this Response.

I. Claim Rejections -35 USC § 102(b)

The Office Action has rejected 1-5 and 10-24 under 35 U.S.C. § 102(b) as being as being anticipated by Zalewski et al., US Patent No. 6260068 B1 (Zalewski). However, the Office Action has failed to meet its burden of makings a prima facie case of anticipation for the claims, and such rejections should be withdrawn.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim.*" *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added). Zalewski simply fails to disclose every aspect of the inventions claimed in Claims 1-5 and 10-24. The Examiner has therefore failed to meet his burden of making a prima facie case of anticipation.

At paragraph 3 of the Application, Applicants disclose a HyperThreaded system.

> In another type of processor based system such as that depicted in Fig. 1c, a hardware processor that maintains separate architectural states in the processor's hardware for ***a plurality of logical processors*** may, however, have ***a single processor core pipeline that is shared by the logical processors and a single set of processor execution resources, including the TLB, that is shared by the logical processors***. Such a processor architecture is exemplified by the Intel® Xeon™ processor with Hyper Threading Technology, among others, and is well known in the art.

(emphasis added). Such system includes multiple logical processors that share the execution resources of a single core. Zalewski does not disclose, suggest nor teach such a system. In

particular, Zalewski does not disclose, teach nor suggest "a plurality of logical processors of a single physical processor share processor execution resources of the single physical processor" (amended Claim 1, in part). A prima facie case of anticipation has thus not been made with respect to Claim 1, and claim 1 should therefore be allowed.

As suggested by the Examiner, Claim 10 now recites "a single physical processor that implements a plurality of logical processors" (Claim 10, in part). Zalewski does not teach, suggest nor disclose such limitation. For at least this reason, a prima facie case of anticipation has not been made with respect to Claim 10. Claim 10 is therefore allowable for at least this reason. In addition, Claims 11-14, which depend from Claim 10, are also allowable.

Claim 15 recites "a physical processor" and "a plurality of logical processors implemented in the physical processor;" (Claim 15, in part). Zalewski does not teach, suggest nor disclose such limitation. For at least this reason, a prima facie case of anticipation has not been made with respect to Claim 15. Claim 15 is therefore allowable for at least this reason. In addition, Claims 16-19, which depend from Claim 15, are also allowable.

Amended Claim 20 recites, in part, "a plurality of logical processors implemented in a single physical processor share processor execution resources of the physical processor" (Claim 20, in part). ***Zalewski does not teach, suggest nor disclose such limitation. For at least this reason, a prima facie case of anticipation has not been made with respect to Claim 20. Claim 20 is therefore allowable for at least this reason. In addition, Claims 21-28, which depend from Claim 20, are also allowable. It should be noted that the limitation of "logical processors" is already present in previously presented Claims 10 and 15. Accordingly, no new search should be required for this amendment to Claim 20.

I. Claim Rejections -35 USC § 103(a)

The Office Action has rejected 6-9 and 25-28 under 35 U.S.C. 103(a) as unpatentable over Zalewski et al., US Patent No. 6260068 B1 (Zalewski). However, the Office Action has failed to meet its burden of makings it prima facie case of obviousness for the claims, and such rejections should be withdrawn.

The legal requirements for a prima facie case of obviousness are clear. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when the prior art reference (or references when combined) teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

However, Applicant notes that the rejections of the claims under 35 USC 103(a) rely on the above discussed rejections of claims 2 as anticipated by Zalewski. Therefore because the rejections of claims 1 and 20 cannot stand, as argued previously, the rejections of claims 6-9 and 25-28 also cannot stand for at least this reason and should be withdrawn.

Applicant reserves the right to argue other assertions made in rejecting these claims in the future.

Therefore as argued above, the rejections of all claims pending in the application, i.e. claims 1-28, should withdrawn and the claims allowed.

The Examiner is welcome to contact the Attorney of Record, Shireen Irani Bacon (Reg. No. 40,494) at 512.263.1250 to discuss any matters with the case. The Commissioner is hereby authorized to charge any fees in connection with this communication to our Deposit Account No.50-0221.

Respectfully submitted,

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